REMARKS

Claims 1, 3-12 and 22-23 are rejected under 35 USC 103(a) as being unpatentable over AAPA and further in view of Fujii, US Patent No: 5,898,695

The applicant respectfully asserts that independent claims 1 and 22 of the present invention should not be found unpatentable over AAPA and further in view of Fujii because neither Fujii nor the AAPA teach all the claimed limitations of the present invention and the differences would not be obvious to a person skilled in the art without further inventive process. There are at least three reasons provided in the below paragraphs of why claims 1 and 22 should be found allowable with respect to the cited references.

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1. Slave to host data transmission

Firstly, in contrast to the present invention, the technology of the prior art involves doing a DMA controlled data transmission to RAM. Concerning the rejections of the Examiner in the Office action of 12/31/2007, with reference to Figure 5 of Fujii, the transfer buffer 141 of the prior art of Fujii is interpreted by the Examiner as being equivalent to the slave unit of the present invention. Likewise, the DMA controller 121 of the prior art is interpreted to be equivalent to the host of the present invention. Note that these interpretations are clearly specified by the Examiner on page 3, points (a) and (b) of the Examiners rejections in view of the Fujii reference.

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In the prior art of Fujii, the transfer buffer 141 and the DMA controller 121 transmit commands between themselves. But after the commands are transmitted, the transfer buffer 141 sends the data directly to a RAM 7, which is not within the DMA controller 121. For example, please refer to Figure 5 showing the transfer buffer 141, the DMA controller 121, and the RAM 7 all being separate units.

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However, claim 1 of the present invention states:

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"(a) the slave chip informing the host chip of data needed to be transmitted;

- (b) when being informed by the slave chip, the host chip informing the slave chip to start to transmit the data; and
- (c) when being informed by the host chip, the slave chip starting to transmit the data to the host chip." (present invention claim 1 emphasis added)

Therefore, the applicant respectively points out that, in the prior art of Fujii, the transfer buffer 141 (the slave) does not transmit data to the host (DMA controller 121). Instead the data is transferred directly to a RAM 7. This operation is different than the present invention, in which a slave transfers data to a host chip. For example, refer to step (c) of claim 1 of the present invention quoted above. For at least the reason that Fujii does not teach step (c) of claim of the present invention, the applicant asserts that claim 1 should be found allowable. A similar argument also applies to independent claim 22.

15 2. Servo functionality

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Secondly, the prior art does not mention or teach any servo or related functional element. Both the prior art and the AAPA do not mention or suggest any DMA buffer control. The applicant continues to have trouble understanding how the Examiner can account for the fact that the prior art (AAPA and Fujii) do not mention any servo providing data to a processor but still reject the present application that claims exactly this structure.

3. Removal of host involvement by prior art

Finally, the prior art protection scope involves performing a DMA transfer to eliminate involvement of (and all assistance required by) a processor. However, the present invention claims having a slave chip requesting a host chip to accept a command, and then the slave chip transmitting data to the host chip. In this way, the technology claimed by the present invention is clearly different than that of the prior art. That is, in the prior art, the host (processor) involvement is eliminated by the DMA; however, in the present invention, the

Appl. No. 10/709,551 Amdt. dated March 17, 2008

Reply to Office action of December 31, 2007

slave chip transfers data to the host chip. That is, the host is still involved in the data transfer, unlike the teachings of Fujii.

In summary, for at least the following three reasons, the applicant respectfully asserts that the present invention as claimed in independent claims 1 and 22 should be found allowable with respect to the AAPA, Fujii and Satoh.

- 1. The prior art of Fujii does not teach or suggest the slave chip (transfer buffer 141) transmitting data to the host chip (DMA controller 121) as is claimed in the present invention.
- 2. No servo or related item is mentioned by the prior art in contrast to what is claimed in the present invention.
 - 3. The prior art technology of removing all assistance by a processor is different than that of the present invention, which involves a slave chip transmitting data to a host chip after the host chip accepts a command from the slave chip.

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Claims 2-21 and 23-28 are dependent claims and should be found allowable for at least the same reasons as their respective base claims. Reconsideration of claims 1-28 is respectfully requested.

Claims 2, 13-21 and 24-28 are rejected under 35 USC(a) as being unpatentable over AAPA and Fujii and further in view of Satoh et al, US Pub No: 2003/0128702

As previously stated, claims 2, 13-21 and 24-28 are dependent claims being dependent upon base claims being allowable according to the above stated arguments. For this reason, dependent claims 2, 13-21 and 24-28 should also be found allowable.

25 Reconsideration of claims 2, 13-21 and 24-28 is respectfully requested.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to

Appl. No. 10/709,551 Amdt. dated March 17, 2008

Reply to Office action of December 31, 2007

the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

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Sincerely yours,

Winten Harr	Doto	03/17/2008
<u>* * </u>	Date:	03/17/2008

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is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)